AMENDMENTS TO THE CLAIMS

Listing Of Claims

Claims 1-50 (Canceled)

51. (currently amended) A method for fabricating a semiconductor component comprising:

providing a substrate comprising a plurality of first interconnect contacts and a plurality of second interconnect contacts;

attaching a first die to the substrate in electrical communication with the first interconnect contacts;

forming a first encapsulant comprising a planar surface on the first die and at least one feature on the planar surface configured to facilitate bonding to the first encapsulant;

attaching a second die to the planar surface and to the feature in electrical communication with the second interconnect ~~s~~ contacts; and

forming a second encapsulant on the second die and on the first encapsulant.

52. (previously presented) The method of claim 51 wherein the forming the first encapsulant step comprises molding, and the feature comprises a molded feature.

53. (previously presented) The method of claim 51 wherein the feature comprises a layer of material applied to the surface.

54. (previously presented) The method of claim 51 wherein the feature comprises a molded ridge, dimple, indentation or groove.

55. (currently amended) ~~The method of claim 54 wherein~~

A method for fabricating a semiconductor component comprising:

providing a substrate comprising a plurality of first interconnect contacts and a plurality of second interconnect contacts;

attaching a first die to the substrate in electrical communication with the first interconnect contacts;

forming a first encapsulant comprising a surface on the first die and at least one feature on the surface configured to facilitate bonding to the first encapsulant;

attaching a second die to the surface and to the feature in electrical communication with the second interconnect ~~s~~ contacts; and

forming a second encapsulant on the second die and on the first encapsulant;

the forming the first encapsulant step ~~comprises~~ comprising molding with a mold cavity configured to form the feature and to prevent an encapsulating material from contaminating the second interconnect contacts.

56. (currently amended) The method of claim ~~51~~ 55 further comprising forming a plurality of terminal contacts on the substrate in electrical communication with the first interconnect contacts and the second interconnect contacts.

57. (previously presented) A method for fabricating a semiconductor component comprising:

providing a substrate comprising a plurality of first interconnect contacts and a plurality of second interconnect contacts;

adhesively bonding a first die to the substrate;

electrically connecting the first die to the first interconnect contacts;

encapsulating the first die and the first interconnect contacts in a first encapsulant having a planar surface on the first die and at least one molded feature on the planar surface configured to facilitate bonding to the first encapsulant;

adhesively bonding a second die to the planar surface and to the molded feature;

electrically connecting the second die to the second interconnect contacts; and

encapsulating the second die, the first encapsulant, and the second interconnect contacts in a second encapsulant.

58. (previously presented) The method of claim 57 wherein the encapsulating the first die step comprises transfer molding with a direct gate mold cavity.

59. (previously presented) The method of claim 57 wherein the molded feature comprises a ridge, a dimple, an indentation or a groove.

60. (previously presented) The method of claim 57 further comprising adhesively bonding a third die to the second encapsulant and encapsulating the third die and the second encapsulant in a third encapsulant.

61. (previously presented) The method of claim 57 wherein the adhesively bonding the first die step comprises forming a first adhesive layer between a back side of the first die and the substrate.

62. (previously presented) The method of claim 57 wherein the adhesively bonding the second die step comprises forming a second adhesive layer between the second die and the first encapsulant.

63. (previously presented) A method for fabricating a semiconductor component comprising:

providing a substrate on a leadframe comprising a plurality of first interconnect contacts and a plurality of second interconnect contacts;

back bonding a first die to the substrate comprising a circuit side, a plurality of first die contacts on the circuit side, and a back side;

bonding a plurality of first interconnects to the first die contacts and to the first interconnect contacts;

encapsulating the first die and the first interconnects in a first encapsulant having a planar surface on the circuit side;

back bonding a second die to the planar surface of the first encapsulant comprising a plurality of second die contacts;

bonding a plurality of second interconnects to the second die contacts and to the second interconnect contacts;

encapsulating the second die, the second interconnects and the first encapsulant in a second encapsulant; and

singulating the substrate from the leadframe such that the second encapsulant and the substrate have a matching peripheral outline.

64. (previously presented) The method of claim 63 wherein the second interconnect contacts are located proximate to a peripheral edge of the substrate and the second interconnect contacts are located proximate to an inner portion of the substrate.

65. (previously presented) The method of claim 63 wherein the first interconnect contacts and the second interconnect contacts are arranged in spaced rows on opposing edges of the substrate.

66. (previously presented) The method of claim 63 wherein the back bonding the first die step comprises forming a first adhesive layer between the back side of the first die and the substrate.

67. (previously presented) The method of claim 63 further comprising forming at least one molded locking feature on the first encapsulant configured to promote adhesion of the second die to the first encapsulant.

68. (previously presented) The method of claim 63 wherein the first interconnects and the second interconnects comprise wire bonded wires.

69. (previously presented) The method of claim 63 wherein the first interconnects and the second interconnects comprise bonded TAB tape.

70. (previously presented) The method of claim 63 further comprising forming a plurality of terminal contacts on the substrate in electrical communication with the first interconnect contacts and the second interconnect contacts.

71. (previously presented) The method of claim 63 further comprising bonding a third die to the second encapsulant and forming a third encapsulant on the third die and the second encapsulant.

72. (previously presented) The method of claim 63 wherein the encapsulating the first die step comprises transfer molding with a direct gate mold cavity.

73. (previously presented) The method of claim 63 wherein the encapsulating the first encapsulant step comprises molding at least one locking feature on the first

encapsulant configured to facilitate bonding of the second die to the first encapsulant.

74. (previously presented) The method of claim 63 wherein the encapsulating the first die step comprises injection molding.

75. (previously presented) The method of claim 63 wherein the encapsulating the first die step comprises deposition of a viscous plastic through a nozzle.

76. (previously presented) The method of claim 63 wherein the encapsulating the first die step comprises stereo lithography.

77. (currently amended) A method for fabricating a semiconductor component comprising:

providing a substrate comprising a plurality of interconnect contacts and a plurality of terminal contacts in electrical communication with the interconnect contacts;

forming a plurality of die stacks on the substrate, each die stack comprising a first die bonded to the substrate in electrical communication with the interconnect contacts, a first encapsulant encapsulating the first die comprising a planar surface on the first die and at least one feature on the planar surface configured to facilitate bonding to the first encapsulant, and a second die bonded to the first encapsulant in electrical communication with the interconnect contacts; and

forming a second encapsulant on the substrate encapsulating the die stacks;

the forming the die stacks step comprising wire bonding the first die and the second die to the interconnect contacts.

78. (currently amended) The method of claim 77 wherein the forming the second encapsulant step comprises molding.

~~die stacks step comprises wire bonding the first die and the second die to the interconnect contacts.~~

79. (currently amended) ~~The method of claim 77 wherein~~

A method for fabricating a semiconductor component comprising:

providing a substrate comprising a plurality of interconnect contacts and a plurality of terminal contacts in electrical communication with the interconnect contacts;

forming a plurality of die stacks on the substrate, each die stack comprising a first die bonded to the substrate in electrical communication with the interconnect contacts, a first encapsulant encapsulating the first die comprising a planar surface on the first die and at least one feature on the planar surface configured to facilitate bonding to the first encapsulant, and a second die bonded to the first encapsulant in electrical communication with the interconnect contacts; and

forming a second encapsulant on the substrate encapsulating the die stacks;

the forming the die stacks step ~~comprises~~ comprising TAB bonding the first die and the second die to the interconnect contacts.

80. (currently amended) ~~The method of claim 77 wherein~~

A method for fabricating a semiconductor component comprising:

providing a substrate comprising a plurality of interconnect contacts and a plurality of terminal contacts in electrical communication with the interconnect contacts;

forming a plurality of die stacks on the substrate, each die stack comprising a first die bonded to the substrate in electrical communication with the interconnect contacts, a first encapsulant encapsulating the first die comprising a planar surface on the first die and at least one feature on the planar surface configured to facilitate bonding to the first encapsulant, and a second die bonded to the first encapsulant in electrical communication with the interconnect contacts; and

forming a second encapsulant on the substrate encapsulating the die stacks;

the forming the die stacks step ~~comprises~~ comprising transfer molding the first encapsulant with a direct gate mold cavity configured to not contaminate selected interconnect contacts.

81. (previously presented) A method for fabricating a semiconductor component comprising:

providing a substrate comprising a plurality of interconnect contacts and a plurality of terminal contacts in electrical communication with the interconnect contacts;

back bonding a first die to the substrate;

electrically bonding the first die to the interconnect contacts;

encapsulating the first die in a first encapsulant;

back bonding a second die to the first encapsulant, the first encapsulant comprising at least one feature configured to facilitate bonding of the second die to the first encapsulant;

electrically bonding the second die to the interconnect contacts;

encapsulating the second die in a second encapsulant;

back bonding a third die to the second encapsulant;

electrically bonding the third die to the interconnect contacts; and

encapsulating the third die and the second encapsulant in a third encapsulant.

82. (previously presented) The method of claim 81 wherein the encapsulating the first die step comprises injection molding the first encapsulant with the feature.

83. (previously presented) The method of claim 81 wherein the electrically bonding the first die step, the electrically bonding the second die step, and the electrically bonding the third die step comprise wire bonding.

84. (previously presented) The method of claim 81 wherein the electrically bonding the first die step, the electrically bonding the second die step, and the electrically bonding the third die step comprise TAB bonding.

85. (previously presented) A system comprising:

a substrate comprising a plurality of interconnect contacts and a plurality of terminal contacts in electrical communication with the interconnect contacts; and

a die stack on the substrate comprising a first die bonded to the substrate in electrical communication with the interconnect contacts, a first encapsulant encapsulating the first die comprising a planar surface on the first die and a molded feature on the planar surface configured to facilitate bonding to the first encapsulant, a second die bonded to the planar surface and to the molded feature in electrical communication with the interconnect contacts, and a second encapsulant encapsulating the second die and the first encapsulant.

86. (previously presented) The system of claim 85 further comprising a plurality of die stacks on the substrate.

87. (previously presented) The system of claim 85 wherein the substrate is contained in a computer.

88. (previously presented) The system of claim 85 wherein the substrate is contained in a camcorder.

89. (previously presented) The system of claim 85 wherein the substrate is contained in a camera.

90. (previously presented) The system of claim 85 wherein the substrate is contained in a cell phone.

91. (previously presented) The system of claim 85 wherein the substrate is contained in a medical device.

92. (previously presented) The system of claim 85 wherein the first encapsulant comprises at least one locking feature configured to increase adhesive bonding of the second die to the first encapsulant.

93. (previously presented) The system of claim 85 wherein the die stack comprises a third die bonded to the second encapsulant, and a third encapsulant encapsulating the third die and the second encapsulant.

94. (previously presented) The system of claim 85 wherein the molded feature comprises a ridge, a dimple, an indentation or a groove.

95. (previously presented) The system of claim 85 wherein the substrate and the die stack comprise a multi chip module.